PERFORMANCE BENCHMARKING OF CRYO-CMOS EMBEDDED SRAM AND DRAM IN 40NM CMOS TECHNOLOGY

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Abstract

The interface electronics needed for quantum processors require cryogenic CMOS (cryo-CMOS) embedded digital memories covering a wide range of specifications. To identify the optimum architecture for each specific application, this article presents a benchmark from room temperature (RT) down to 4.2 K of custom SRAMs/DRAMs in the same 40-nm CMOS process. To deal with the significant variations in device parameters at cryogenic temperatures, such as the increased threshold voltage, lower subthreshold leakage, and increased variability, the feasibility of different memories at cryogenic temperature is assessed and specific guidelines for cryogenic memory design are drafted. Unlike at RT, the 2T low-threshold-voltage (LVT) DRAM at 4.2 K is up to 2× more power efficient than both SRAMs for any access rate above 75 kHz since the lower leakage increases the retention time by 40 000×, thus sharply cutting on the refresh power and showing the potential of cryo-CMOS DRAMs in cryogenic applications.

Key Words: Cryogenic CMOS (cryo-CMOS), DRAM, eDRAM, memory, quantum computing, SRAM.

I. INTRODUCTION

QUANTUM computers (QCs) can deliver an exponential speedup for several computational problems [1],[2],[3],[4],[5],[6]. However, scaling up the number of quantum bits (qubits) to the thousands or millions necessary for useful computations requires an impractical amount of wires connecting the cryogenic qubits to the room-temperature (RT) control electronics. To overcome such an interconnect bottleneck, electronics integrated in commercial CMOS technology but operating at cryogenic temperature, i.e., cryogenic CMOS (cryo-CMOS), has been proposed [7], [8]. As the power consumption of the cryo-CMOS control electronics must be kept below the cooling power of the cryogenic refrigerators adopted in QC applications, designing power-efficient cryo-CMOS circuits is crucial. The control electronics consist of analog/RF circuits directly interfacing with the qubits to perform operations and measurements, in combination with the digital system-on-chip (SoC) for scheduling the quantum-algorithm execution [9] and processing a large amount of measurement results, e.g., as required for quantum error correction [10], [11], [12], [13], [14]. In modern digital systems, significant fractions of the area and power are consumed by the memory, thus making the optimization of cryo-CMOS embedded memories essential. However, accurately estimating the power consumption of a memory at cryogenic temperatures is challenging due to the lack of reliable cryogenic device models.

a. Cryo-CMOS Device Behavior

Cooling down to cryogenic temperatures affects the characteristics of short-channel NMOS and PMOS transistors by increasing their threshold voltage V_{th} (100–200 mV), subthreshold slope (∼3× steeper), and carrier mobility (∼2× for low-field mobility).

Additionally, the mismatch between devices increases, as shown in [62] and [63] for 40-nm bulk CMOS and 28-nm bulk CMOS, respectively, interconnect resistance drops (∼30%) [64], and the capacitance of source/drain junctions decreases due to wider depletion regions due to freeze-out [19]. For analog circuits, this results in an increased bandwidth and reduced power consumption. For full-swing digital circuits, the mobility increase compensates the effects of the larger V_{th} and, together with the reduced resistance and capacitance, results in a speed-up for digital circuits from 10% to 20% for 40-nm bulk CMOS [65], [66], [67]. For more advanced technology nodes, the speed-up from RT to 4.2 K is reduced due to the increased relative importance of interconnect capacitance and lower supplies,

enhancing the relative V_{th} increase [65]. However, the speed- up could be recovered for F in FET technologies by scaling V_{th} [40]. The increased V_{th} and the steeper subthreshold slope lead to severely reduced subthreshold leakage, while gate leakage stays approximately constant (<2× smaller) [68]. For these digital circuits, this will result in greatly reduced leakage power, while keeping the dynamic power consumption similar.

II. EXISTING METHOD

In the existing system technique with configurable multiple boost planes to implement low-power 6T SRAM. Measurement results show that the proposed 6T SRAM demonstrated stable performance from room temperature to 6 K, achieving extremely low minimum operating voltages of 0.23V and 0.31V at room temperature and 6 K, respectively. Despite the optimization of power consumption, more research works focused on improving memory density. Presenting a 6T SRAM Cell Analysis in Various Technologies to analyse the Static Noise margin of the cell. Together with the read channel's isolation from the real internal storage nodes, this takes out the read-disturbance. Additionally, it uses a write-assist mechanism to carry out its write operation in pseudo differential form using a write bit line and control signal[1]. In this study, a 6T SRAM cell for 90nm and 180nm technologies has been created. The Cadence Virtuoso tool has been applied to modelling and design. Using nmos1V and nmos2V cells in 180nm and 90nm technologies, the static noise margin for SRAM has been determined. SNM decreases with shrinking technology, as expected, and CMOS 1v transistors have been found to have better SNM than CMOS2v transistors [1].

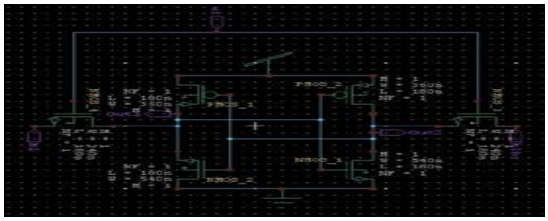

Figure: Existing System

III. DESIGN METHODLOGY

In the proposed system Memory Circuits Volatile and non-volatile memories are two major categories of CMOS-based memory. Volatile memories, such as static random-access memory (SRAM) and dynamic RAM (DRAM), exhibit improved performance metrics at cryogenic temperatures due to reduced leakage currents and enhanced carrier mobility. Additionally, the high compatibility of volatile memory with silicon-based CMOS processes facilitates achieving high levels of integration. Due to its data stability and high-speed advantages, SRAM has become the most widely used memory topology.

proposed a 4T SRAM structure optimized for operation at 77 K by eliminating two pMOS transistors from the pull-up network. The 4T SRAM achieved a reduction of cell area by 20.3%, compared to the standard 6T SRAM structure. Moreover, it also provided faster read and write operations. Compared to SRAM, DRAM can achieve higher density due to its compact bitcell layout. However, DRAM requires frequent refresh operations to maintain data correctness, resulting in extra area and power overhead.

The additional costs associated with DRAM make it less attractive for memory implementation at room temperature. Benefiting from the optimized leakage current and carrier mobility at cryogenic temperature, the data retention time and read/write operations of DRAM can be further improved. Recent research works have explored various DRAM topologies for cryogenic operations. Chakraborty et al. [44] proposed a pseudo-static 1T capacitorless (1T0C) DRAM using 22 nm fully depleted silicon-on-insulator (FDSOI) technology at 4.8 K, named Cryo-DRAM.

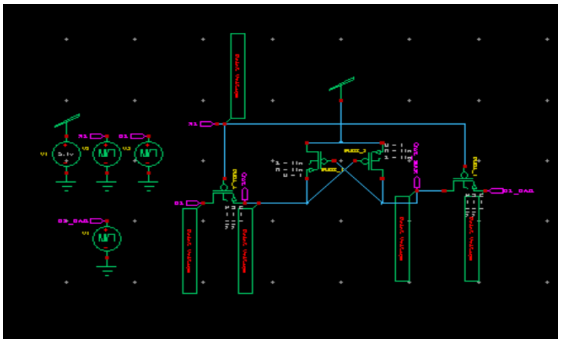

Figure: Proposed System

proposed a 4T CSDB-eDRAM design with dual-port read topologies and ensure disturb-free read operations. The 4T CSDB-eDRAM achieved an impressive data retention time of 16.67s at 4.2 K,

with a maximum frequency of 1.41GHz. The studies above have demonstrated significant improvements in the performance of various SRAM and DRAM cells at cryogenic temperatures a comprehensive benchmark from room temperature down to 4.2 K of custom memory cells, including 6T SRAM, 2T NWPR (nMOS for write and pMOS for read), 3T NWPR, and 3T NRPW (nMOS for read and pMOS for write) in the same 40 nm CMOS process. Measurement results showed that the 2T low-threshold-voltage (LVT) DRAM operating at 4.2 K is up to twice as energy-efficient as SRAM for access rates exceeding 75 kHz. These findings underscore the potential of cryogenic DRAMs for cryogenic applications.

IV. SIMULATION RESULTS

The entire simulation and result obtaining using test vectors are done with the help of Tanner 16.1 software.

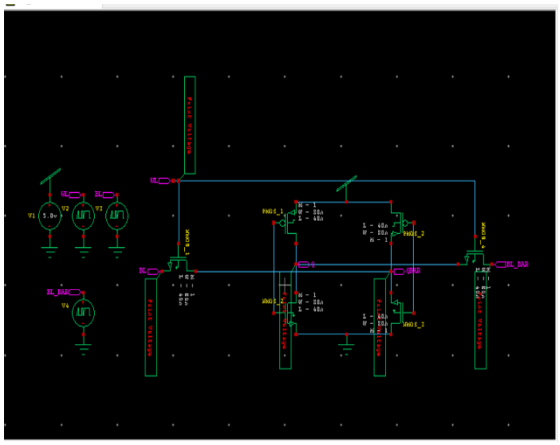

Figure: 6T SARM Existing System Diagram

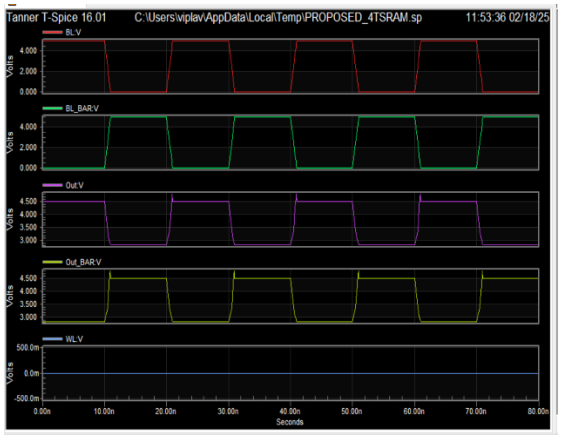

Figure – 8: 6T SARM Existing System Simulation Outputs

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Power Results

VV2 from time 0 to 1e-008
Average power consumed -> 1.475947e+001 watts
Max power 1.475947e+001 at time 0
Min power 1.475947e+001 at time 0

VV3 from time 0 to 1e-008
Average power consumed -> 1.812614e-003 watts
Max power 1.812614e-003 at time 0
Min power 1.812614e-003 at time 0

VV4 from time 0 to 1e-008
Average power consumed -> 0.000000e+000 watts
Max power 0.000000e+000 at time 0
Min power 0.000000e+000 at time 0
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Figure: 6T SRAM Existing System Power Results

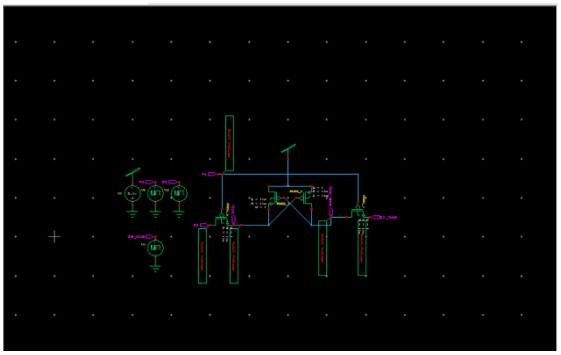

Figure: 4T SRAM Proposed system Circuit

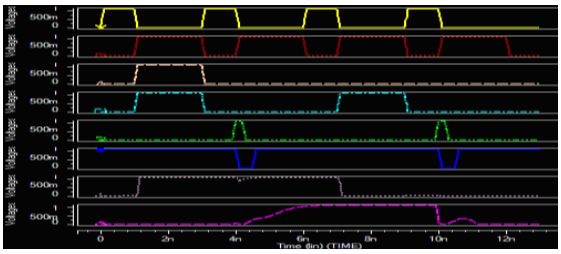

Figure: 4T SRAM Wave forms

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Min power 0.000000e+000 at time 0

VV3 from time 0 to 8e-008
Average power consumed -> 9.968859e-002 watts
Max power 2.094245e-001 at time 3e-008
Min power 0.000000e+000 at time 1.1e-008

VV4 from time 0 to 8e-008
Average power consumed -> 9.649796e-002 watts
Max power 2.094245e-001 at time 4e-008
Min power 0.000000e+000 at time 0


Parsing                         0.01 seconds
Setup                           0.01 seconds
DC operating point              0.05 seconds
Transient Analysis              0.04 seconds
Overhead                        0.64 seconds
```

Figure: 4T SRAM Power Results

V. CONCLUSION

By comparing single-bank static and dynamic memories at cryogenic temperature, this article

shows that well-designed dynamic memories can outperform static memories for middle-to-high frequency applications in terms of area and power. While the subthreshold leakage reduces substantially from RT to 4.2 K, gate leakage stays approximately constant, thus still limiting the retention time. Still, adopting dynamic cells with enhanced resistance to gate leakage and cryogenic Vth shifts can significantly increase retention time, thus lowering the refresh power. The increased variability in both cells and peripherals may increase the number of outlier cells, while the lower noise reduces the read error rate. Embracing the design guidelines outlined here for cryogenic embedded memories will facilitate the adoption of dynamic-memory cells for high-density low-power cryogenic memories, thereby enabling the complex cryo-CMOS SoCs needed in future QCs.

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